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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,432	12/15/2000	Jun Souk Joung	HI-023	8762

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EXAMINER	
DELGADO, MICHAEL A	
ART UNIT	PAPER NUMBER
2144	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,432	JOUNG, JUN SOUK	
	Examiner	Art Unit	
	Michael S. A. Delgado	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 10-11 and 15-20* is/are rejected.

7)☒ Claim(s) *6-9,12-14 and 21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "IPC" in claims 1 and 16 are used by the claim to mean "information processing code", while the accepted meaning is "interprocessor communication." The term is indefinite because the specification does not clearly redefine the term. The definition according to Webopedia is: "A capability supported by some operating systems that allows one *process* to communicate with another process. The processes can be running on the same computer or on different computers connected through a network. IPC enables one application to control another application, and for several applications to share the same data without interfering with one another. IPC is required in all multiprocessing systems, but it is not generally supported by single-process operating systems such as DOS. OS/2 and MS-Windows support an IPC mechanism called DDE."

Response to Arguments

In response to the argument that the IPC format is not taught by the prior art. In the prior art a controller 200 (upper processor) is used to configure a group of DSPs (lower processors) (111, 112, and 113) (Col 4, lines 40-55). The communication that takes place between upper

processor and lower processors is consistent with the definition of an IPC operation, which has to be in an IPC format.

In response to the argument that the grouping of the lower processors with a representative address is not taught by the prior art. In figure 4 of the prior art a "common boot address" is used to simultaneously download DSP111, DSP112 and DSP 113. The source for the download data is from a master ROM 230 and for the DSPs to load simultaneously from a single source the address presented to the DSPs has to be the same which is consistent with the group representative address that is being claimed by the applicant.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 10-11 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No 6,401,200 by Nishiike et al.

In claim 1, Nishiike teaches about a method for down-loading data from an upper processor "Controller" to a plurality of lower processors "DSPs" of a mobile communications switching system in a process of resetting the processors, the method comprising (Col 1, lines 5-15) (Fig 3):

requesting an information download from the lower processors to the upper processor (Col 1, lines 5-15); (Boot process initiated by DSPs)

accessing a memory of the upper processor "master ROM" containing the requested information down-load (Col 4, lines 20-30);

determining whether the accessed information has an error (Col 4, lines 20-30); (ROM has built in parity error checking).

grouping the lower processors with a representative address "Common boot address" (Col 2, lines 55-67) (Fig 4); and

creating the accessed information in an IPC format (Communication between processors – Controller and DSPs) and transferring the IPC format information by using the group representative address (Col 2, lines 55-67).

In claim 2, Nishiike teaches about a method of claim 1, wherein the resetting of the processors includes an initial loading and a re-loading (Col 5, lines 30-40).

In claim 3, Nishiike teaches about a method of claim 1, wherein the group representative address includes all the lower processors (Fig 4)

In claim 4, Nishiike teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping the plurality of lower processors using the group representative address "Common boot address" (Fig 4).

In claim 5, Nishiike teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping at least one additional lower processor (Fig 4).

In claim 10, Nishiike teaches about a method for downloading data from a first processor "Controller" to a plurality of second processors "DSPs" while resetting the processors, the method comprising (Col 1, lines 5-15) (Fig 3):

transmitting a request for an information download from the plurality of second processors to the first processor (Col 1, lines 5-15); (Boot process initiated by DSPs)

accessing once a memory of the first processor for the requested information;

grouping the second processors using a prescribed processor address (Col 4, lines 20-30); and

assembling the accessed information in a prescribed format and transferring the assembled requested information to at least two second processors using a group representative address (Col 2, lines 55-67)

In claim 11, Nishiike teaches about a method of claim 10, wherein the grouping of the plurality of lower processors is performed using the group representative address (Fig 4).

In claim 15, Nishiike teaches about a method of claim 10, wherein the method further comprises determining whether the accessed requested information has an error (Col 4, lines 20-30). (ROM has built in parity error checking).

In claim 16, Nishiike teaches about a mobile communications switching method comprising (Fig 3):

requesting information from a first processor "Controller" (Col 1, lines 5-15) (Fig 3);

grouping a plurality of second processors "DSPs" using a representative address of the plurality of second processors(Col 1, lines 5-15) (Col 2, lines 55-67);

providing the requested information in an information processing code (IPC) format (Col 2, lines 55-67); and

transferring the requested information in the IPC format based on the representative address of the plurality of second processors (Fig 4).

In claim 17, Nishiike teaches about a method of claim 16, further comprising accessing a memory of the first processor having the requested information (Col 5, lines 5-10) .

In claim 18, Nishiike teaches about a method of claim 17, further comprising determining whether the requested information has an error (Col 4, lines 20-30); (ROM has built in parity error checking).

In claim 19, Nishiike teaches about a method of claim 16, wherein the method is provided in a process of resetting the second processors (Col 4, lines 40-50). (In order to prevent corruption of the configuration data, a boot process has to be preceded by a reset in this way the device will be placed in a known state prior to being boot)

In claim 20, Nishiike teaches about a method of claim 19, wherein the resetting of the second processors includes an initial loading and a re-loading (Col 5, lines 30-40).

Allowable Subject Matter

3. Claims 6-9, 12-14 and 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: prior art failed to teach about using a representative address that comprises a node address (NA), a BHIU address (BA), a cinu address (CA), and a slot address (SA).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,212,557 by Oran teaches about a method and apparatus for synchronizing upgrades in distributed network data processing systems.

US Patent 6,021,442 by Ramanan et al, teaches about a method and apparatus for partitioning an interconnection medium in a partitioned multiprocessor computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. A. Delgado whose telephone number is 703-305-8057. The examiner can normally be reached on 7.30 AM - 5.30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WILLIAM A CUCHLINSKI JR can be reached on (703)308-3873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MD

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